Amendments to the Specification:

Rewrite the paragraph at page 2, line 21 as follows:

Referring to Figure 2, there is a hysteresis curve corresponding to the ferroelectric capacitor 100. The hysteresis curve includes net charge Q or polarization along the vertical axis and applied voltage along the horizontal axis. By convention, the polarity of the ferroelectric capacitor voltage is defined as shown in Figure 1. A stored "0", therefore, is characterized by a positive voltage at the plateline terminal with respect to the access transistor terminal. A stored "1" is characterized by a negative voltage at the plateline terminal with respect to the access transistor terminal. A "0" is stored in a write operation by applying a voltage Vmax across the ferroelectric capacitor. This stores a saturation charge Qs in the ferroelectric capacitor. The ferroelectric capacitor, however, includes a linear component in parallel with a switching component. When the electric field is removed, therefore, the linear component discharges and only the residual charge Qr remains in the switching component. The stored "0" is rewritten as a "1" by ~~applying Vmax to~~ reversing the polarity of Vmax across the ferroelectric capacitor. This charges the linear and switching components of the ferroelectric capacitor to a saturation charge of –Qs. The stored charge reverts to –Qr when the voltage across the ferroelectric capacitor is removed. Finally, coercive points V_C and $-V_C$ are minimum voltages on the hysteresis curve that will degrade a stored data state. For example, application of V_C across a ferroelectric capacitor will degrade a stored "1" even though it is not sufficient to store a "0". Thus, it is particularly important to avoid voltages near these coercive points unless the ferroelectric capacitor is being accessed.

Rewrite the paragraph at page 9, line 4 as follows:

During a read cycle, the timing and control circuit receives high level signals EN on lead 614 and R/W on lead 612 and an 18-bit address on bus 608. A row decoder circuit 702, a plate decoder circuit 706, and a column decoder circuit 704 are coupled to receive respective address bits from bus 608. Responsively, the FRAM array produces a plurality of data bits that are received and

amplified by sense amplifiers 708. Column decoder circuit 704 selects one 32-bit data word from sense amplifiers 708 in response to the column address bits on bus 608. This selected 32-bit data word is applied to output circuit 712. Output circuit 712 further amplifies the data word on data bus 610 to overwrite a data location in CAM 602 indicated by address table pointer ~~806~~ 880 (Figure 8) as will be described in detail.

Rewrite the paragraph at page 12, line 19 as follows:

Referring back to Figure 8 together with Figure 10, termination of the initial access cycle will be described in detail. Address transition detector 830 receives initial address transition signals 1000 and produces a high level address transition signal 1002 for a short time after the address signals are stable. No match is detected on the initial access cycle whether read or write. Match lead signal LMAT on lead 836, therefore, is held low 1012 by address flag bit 826 as previously described. NOR gate 838 and OR gate 868 respectively produce high level enable signals EN* on lead 860 and EN 1014 on lead 614. A low level pulse ATD* 1006 (on lead 834 at Figure 8) is produced by the falling edge 1004 of signal ATD. This low level pulse ATD* is applied to the gate of P-channel transistor 1400 (on lead 834 at Figure 14) of latch circuit L0. Accordingly, P-channel transistor 1400 pulls match lead signal LMAT high 1018. Inverter 1404 subsequently produces a low level signal at the gate of P-channel transistor 1402, thereby latching lead match signal LMAT high. The high level of signal LMAT drives enable signal EN low 1014. The falling edge of enable signal EN* is applied to NOR gate 854 to produce a high level 1016 increment signal INC on lead 856. This high level increment signal INC increments the 5-bit address table pointer to point to the second address table word A1. The falling edge of enable signal EN applied to inverter 850 produces a high level signal at delay stage 852. After a time delay Δt, the delay stage 852 applies a high level input signal to NOR gate 854, thereby terminating the increment pulse INC and the initial access cycle.

Rewrite the paragraph at page 16, line 9 as follows:

A write cycle where the CAM 602 successfully matches the address on bus 608 with an address stored in the address table differs slightly from the previously described operation. Referring back to Figure 11, when one of the address table words matches the external address on bus 608, one of the lead match signals LMAT 1024 will remain at a high level. This high level applied to NOR gate 838 produces a low level enable signal EN* on lead 860. Address table decode circuits such as AND gate 808, therefore, are not enabled via AND gate 802. Thus, all address word line AWL signals remain low and the contents of the address table remain unchanged. The low level of read/write signal R/W on lead 612 produces a high level signal from inverter 862. This high level signal from inverter 862 and the high level of chip enable signal CE on lead 606 cause AND gate 864 to produce a high level output signal on lead 866. The high level on lead 866 applied to OR gate 868 produces a high level enable signal EN on lead 614. This high level of enable signal EN on lead 614 enables FRAM 604 to produce a data word on bus 610 corresponding to the external address on bus 608. Referring now to Figures 9 and 11, the high level of address transition detector signal ATD on lead 832 together with the high level of lead match signal LMAT on lead 836 produce a low level output signal from NAND gate 900 on lead 904. This low level on lead 904 produces a high level data word line signal DWL on lead 910. The high level data word line signal DWL loads the data word on bus 608 from FRAM 604 into a current data table word indicated by the high level lead match signal LMAT. In the case of a write cycle where an address match is detected, therefore, only the data table word of the CAM designated by lead match signal LMAT is loaded with a new data word from the data bus 610. The matching address table word remains unchanged and the address pointer is not incremented.